Ordering number: EN 3123

CMOS LSI

SANYO No. 3123

LC66E308

4-Bit Single Chip Microcomputer with EPROM

Overview

The LC66E308 is a 4-bit single chip microcomputer with an EPROM on-chip, and can be used for developing and evaluating application programs for the LC6630X series 4-bit single chip microcomputers.
The LC66E308 microcomputer is a 4-bit single chip LSI with an EPROM on-chip and brought to you in ceramic 42-pin dual-in-line package (DIP) form with a window. This window permits the user to erase EPROM program data as many times as he or she wants. Then, it could be said that this single chip LSI is best suited for developing application programs.
The LC66E308 microcomputer has the same function and the pin assignment as those of the 4-bit single chip mask programmed ROM-version LC66308A microcomputer. The on-chip EPROM is 8K bytes in size.

Features

(1) Option functions user-selectable by specifying EPROM option data
The 33 optional functions on the LC6630X series single chip microcomputers can be selected by writing appropriate data to the on-chip EPROM. This function specification by the user allows application system to be developed and tested under the same working environment as that of production chip. In other words, the same interface circuit functions as those of production chips can be built up by the user.
Please note that the above-mentioned optional functions include port output type (open drain or pull-up), output pin logic level at reset, watchdog timer selection and the like.

(2) On-chip 8KB EPROM
The on-chip EPROM enables the user to develop and evaluate application programs which can be run on every LC6630X series microcomputer. Please note that the LC6630X series microcomputers are LC66304A, LC66306A, LC66308A and that they are listed in the table below with a few pieces of information.

(3) Write/Read operation with an EPROM writer
Used with the dedicated writer board (42 pins into 28 pins:W66EP308D), an EPROM writer available on your local market permits the user to write or read data to or from the 8KB on-chip EPROM. Please note that the EPROM writer should be an ADVANTEST product or the EVA850/800 accessory writer used for the 27128 type EPROM. The addresses should be set to 0000H to 2007H.

(4) Pin compatible with a mask programmed ROM-version single chip microcomputer (LC66308A, for example)

(5) Instruction cycle time: 0.92μs to 10μs

(6) Single +5V power supply (Ta = 10 ℃ to 40 ℃)

Configurations

Type Number	Pins	ROM size	RAM size	Package	Remark
LC66304A/306A/308A	42	4K/6K/8KB	512W	DIP42S	under development
LC66E308	42	EPROM8KB	512W	DIC42S with window	under development
LC66P308	42	OTPROM8KB	512W	DIP42S	under development
LC66506B/508B/512B/516B	64	6K/8K/12K/16KB	512W	DIP64S, QIP64	Available
LC66E516	64	EPROM16KB	512W	DIC64S with window	Available
LC66P516	64	OTPROM16KB	512W	DIP64S	under development

The LC66599 (evaluation chip), being an LSI intended for evaluation, should be used with application development tool EVA850/800-TB6630X.

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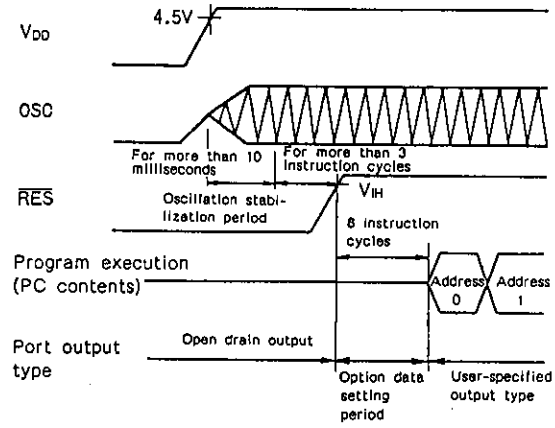
Notes on use

The LC66E308 single chip LSI is intended for use by those who are in charge of the development and evaluation of application programs for the LC6630X series 4-bit single chip microcomputers. Please keep in mind the following items when the user application developers are to work with this single chip microcomputer.

(1) Notes on LC66E308 internal operations after reset

As the figure shows, the LC66E308 microcomputer starts normal program execution at least 3 instruction cycles later after the oscillation by the OSC function block becomes stable. In other words, the $\overline{RES}$ pin level(active low) must be active for at least 3 instruction cycles after the oscillation becomes stabilized. As the figure also shows, the oscillation stabilization requires more than 10 milliseconds. It is also shown that option data setting requires 8 instruction cycles after the $\overline{RES}$ pin level changes to the inactive level (or to V_{IH} voltage level). After all those operations are carried out, the LC66E308 microcomputer starts program execution normally from address 0 in the EPROM (that is, the content at address 0 is automatically set in the program counter (PC)). At this point, please note that port output type will be open drain, not pull-up output type, as long as the $\overline{RES}$ pin stays active. It should be noted that P0, P1 are provided with pull-up resistor.)



(2) Notes on evaluation of user application programs for the LC66304A, LC66306A microcomputers

The above two mask programmed ROM-version microcomputers are equipped with different ROMs in size from that of the LC66E308 microcomputer. Therefore, the following things should be taken into consideration when you are to make an access to the ROM on the LC66E308 microcomputer.

First, it should be kept in mind that the 8 addresses between 2000H and 2007H are used by the user in order to specify functional option data. This 8-byte area is called option specification area. This option specification area must be exclusively used for storing function option data. The option specification will be discussed in detail later in this catalog.

As far as the cross assembler to be employed is concerned, the user should use "LC663S.EXE".

In addition, when you write your user application program, you cannot make any access to addresses beyond the area of a mask programmed ROM. Such addresses cannot exist anywhere on mask programmed ROM-version microcomputers. To avoid such an illegal access to those nonexistent area, it is recommended that jump (or branch) operations with a JMP instruction and so on be used in your user application program. Furthermore, please write "0" to the area beyond that of a mask programmed ROM. In this case, needless to say, the 8 addresses of the EPROM should be excluded from the "0" padding.

(3) Program protection from exposure to light

Exposure to light will destroy the precious EPROM data that you have entered with much labor. In order to protect them, it should be strongly recommended that the EPROM window should be covered with an opaque label while you are at work with the EPROM.

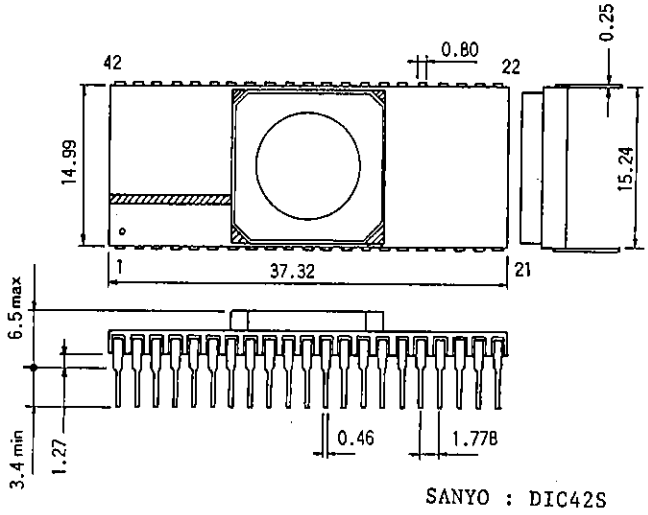
Comparison of LC66E308 and masked ROM version (LC6630X)

Item	LC66E308	Masked ROM version (LC6630X)
Operating supply voltage range (V_{DD})	4.5 to 5.5V	4.0 to 6.0V
Operating free-air temperature (Topg)	+10 to +40 ℃	-30 to +70 ℃
Current dissipation during HALT mode ON (I_{DDHALT})	max. 5mA(4MHz ceramic resonator oscillation) max. 6mA(4MHz external clock source) max. 5mA(RC oscillation)	max. 2.5mA(4MHz ceramic resonator oscillation) max. 3.5mA(4MHz external clock source) max. 2.5mA(RC oscillation)
External RC oscillation time constant Cext Rext	typ 100pF T.B.D	typ 100pF typ 2.7kohm
Port output type at reset	Open drain output type (P0,P1:With pull-up resistor)	User specified output type (selected according to user option data)

(4) For the LC66E308/P308, if the $\overline{RES}$ is set to "L" level during the HOLD mode ($\overline{HOLD}$=L), be sure to change the $\overline{HOLD}$ level from "L" to "H" and then change the $\overline{RES}$ level from "L" to "H" when releasing the HOLD mode.

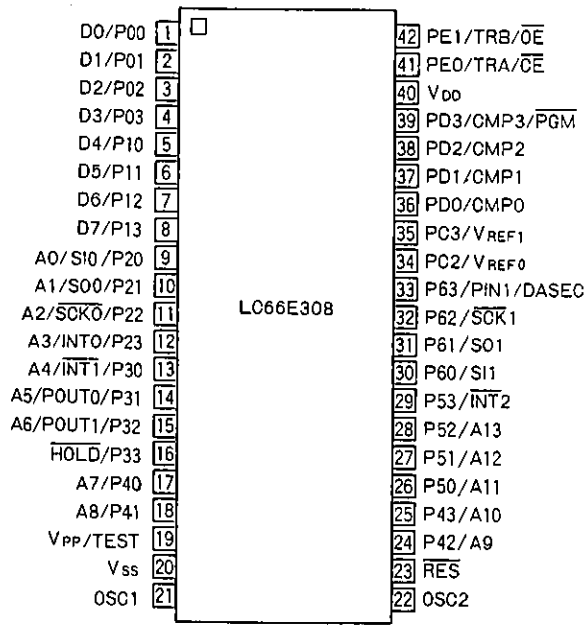
Pin assignment
Case outline 3127-DC42SLSI
(unit: mm)

External dimensions

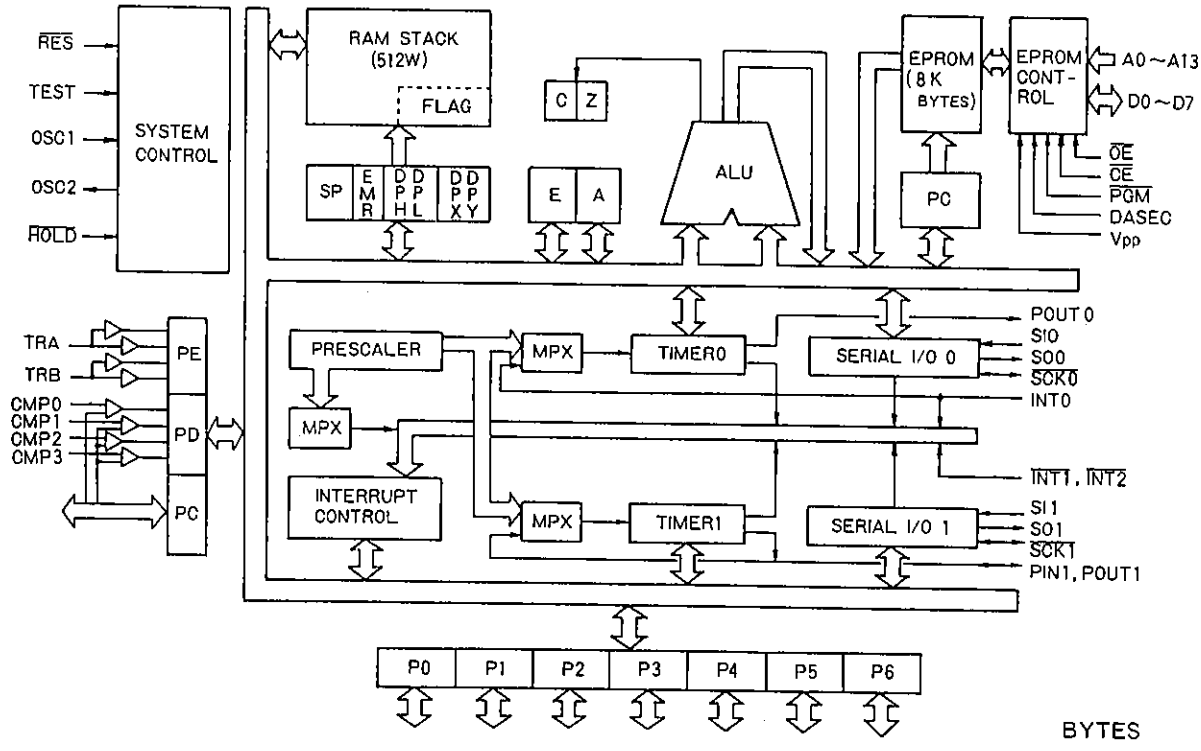


SANYO : DIC42S

DIC42S with a window



System block diagram



Pin description

Pin name	Input/ output	Functional description	Output driver circuit output type	Option	During EPROM mode operation
P00/D0 P01/D1 P02/D2 P03/D3	I/O	Input/output port pins P00 to P03 - Used for input/output operation in 4-bit units or bit units. - Used for controlling HALT mode operation.	- Pch: Pull-up (Pu) MOS type - Nch: Medium sink current output type	- Pull-up (Pu) MOS output type or Nch open drain (OD) output type - Output pin level at reset	Data input/ output pins (D0 to D3)
P10/D4 P11/D5 P12/D6 P13/D7	I/O	Input/output port pins P10 to P13 - Used for input/output operation in 4-bit units or bit units.	- Pch: Pull-up (Pu) MOS type - Nch: Medium sink current output type	- PU MOS output type or Nch OD output type - Output pin level at reset	Data input/output pins (D4 to D7)
P20/SI0/A0 P21/SO0/A1 P22/$\overline{SCK0}$/A2 P23/INT0/A3	I/O	Input/output port pins P20 to P23 - Used for input/output operation in 4-bit units or bit units. - P20: Common with serial input SI0 - P21: Common with serial output S00 - P22: Common with serial clock $\overline{SCK0}$ - P23: Common with INT00 interrupt request input, timer 0-used event count input, pulse width measurement input	- Pch: CMOS type - Nch: Medium sink current output type - +15V withstand voltage at Nch open drain (OD) output	- CMOS output type or Nch OD output type	Address inputs (A0 to A3)
P30/$\overline{INT1}$/A4 P31/POUT0 /A5 P32/POUT1 /A6	I/O	Input/output port pins P30 to P32 - Used for input/output operation in 3-bit units or bit units and for input operation in 4-bit units (together with the P33 pin) or bit units. - P30: Common with $\overline{INT1}$ interrupt request input - P31: Common with burst pulse output from timer 0 - P32: Common with burst pulse output from timer 1 and PWM output	- Pch: CMOS type - Nch: Medium sink current output type - +15V withstand voltage for Nch OD output	- CMOS output type or Nch OD output type	Address input (A4 to A6)
P33/$\overline{HOLD}$	I	HOLD mode control signal input - Used for activating HOLD operation mode with $\overline{HOLD}$ = L (active low) by using a HOLD instruction. - Used for restarting the CPU operation from the HOLD mode operation by changing the $\overline{HOLD}$ pin level from L to H. - Used as input port pin P33 to form a 4-bit input port with P30 to P32. - The CPU blocks cannot be reset even if the RES (active low) pin level changes from H to L, with the $\overline{HOLD}$ pin level = L. This means that you cannot write a user application program requiring the P33/$\overline{HOLD}$ pin to enter the L level state at the moment the system is powered on.			
P40/A7 P41/A8 P42/A9 P43/A10	I/O	Input/output port pins P40 to P43 - Used for input/output operation in 4-bit units or bit units. - These four pins, combined with port pins P50 to P53, can be used for input/output operation in 8-bit units. - These four pins, together with port pins P50 to P53, can be used for 8-bit ROM data output.	- Pch: Pull-up (Pu) MOS type - Nch: Medium sink current output type - +15V withstand voltage for Nch OD output	- PU MOS output type or Nch OD output type	Address input (A7 to A10)
P50/A11 P51/A12 P52/A13 P53/$\overline{INT2}$	I/O	Input/output port pins P50 to P53 - Used for input/output operation in 4-bit units or bit units. - These four pins, combined with port pins P40 to P43, can be used for input/output operation in 8-bit units. - These four pins, together with port pins P40 to P43, can be used for 8-bits ROM data output. - P53: Common with $\overline{INT2}$ interrupt request	- Pch: Pull-up (Pu) MOS type - Nch: Medium sink current output type - +15V withstand voltage for Nch OD output	- Pu MOS output type or Nch OD output type	Address input (A11 to A13)

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Pin name	Input/ output	Functional description	Output driver circuit output type	Option	During EPROM mode operation
P60/SI1 P61/SO1 P62/$\overline{SCK1}$ P63/PIN1 /DASEC	I/O	Input/output port pins P60 to P63 - Used for input/output operation in 4-bit units or bit units. - P60: Common with serial input SI1 - P61: Common with serial output SO1 - P62: Common with serial clock $\overline{SCK1}$ - P63: Common with timer 1-used event count input	- Pch: CMOS type - Nch: Medium sink current output type - +15V withstand voltage for Nch OD output	- CMOS output type or Nch OD output type	
PC2/VREF0 PC3/VREF1	I/O	Input/output port pins PC2 to PC3 - Used for input/output operation in 2-bit units or bit units. - PC2: Common with VREF0 comparator comparison voltage terminal - PC3: Common with VREF1 comparator comparison voltage terminal	- Pch: CMOS type - Nch: Medium sink current type	- CMOS output type or Nch OD output type	
PD0/CMP0 PD1/CMP1 PD2/CMP2 PD3/CMP3 /$\overline{PGM}$	I	Input port pins PD0 to PD3 - These four pins can be programmed for comparator inputs in user application programs. PD0 input will be compared with VREF0. Other inputs will be compared with VREF1. Please note that there are four comparators available in this system and these four comparators are grouped into two (one group: CMP0 and CMP1, the other group: CMP2 and CMP3), and that the comparators must be selected in group units.			EPROM control signal inputs ($\overline{PGM}$)
PE0/TRA/$\overline{CE}$ PE1/TRB/$\overline{OE}$	I	Input port pins PE0 to PE1 - These two tri-state input port pins can be controlled in your application programs.			EPROM control signal inputs ($\overline{OE}$ and $\overline{CE}$)
OSC1 OSC2	I O	Pins for connecting system clock oscillator externally. If external clock source mode is to be employed, use the OSC1 pin only for clock input. Leave the other pin open.		- Ceramic resonator oscillation, RC oscillation or external clock source	
$\overline{RES}$	I	Input port pin for system reset request signal - To initialize the CPU, the $\overline{RES}$ (active low) pin level must be L with the P33/$\overline{HOLD}$ pin level = H.			
TEST/V_{PP}	I	Input port pin for CPU test signal This pin should be connected with the VSS pin when this device is in operation.			V_{PP}
V_{DD} V_{SS}		Power supply pin			

Remarks:

Pu MOS type output --- Pch MOS type transistor acts as a pull-up resistor when data is output.

CMOS type output --- Pch MOS type transistor does not act as a pull-up resistor when data is output. Instead, it forms a complementary-symmetry MOS output circuit with an Nch MOS type transistor.

OD output --- Open drain output type

Note:

At the system reset, the pin output level of each of input/output port pins will be "Floating" except for such pins as ports 0, 1. The output level of these exceptions can be specified by the user options. In addition to this system reset operation, the port output type will be set to open drain at the system reset, which is irrespective of user option specification. In this case, there is no exception. (P0, P1 are provided with pull-up resistor.)

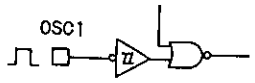
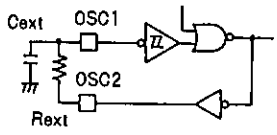
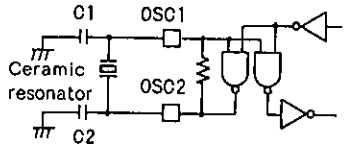
User options

1. Option for specifying the output level of ports 0, 1 at the system reset

   The output level of ports 0, 1 at the system reset can be selected from the following two optional levels by the user option. In this case, it should be kept in mind that the output levels of all the four bits of each input/output port are specified at the same time.

Option name	Condition
1. "H" output level	In 4-bit units
2. "L" output level	In 4-bit units

2. Option for selecting oscillation circuit

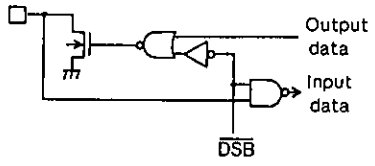
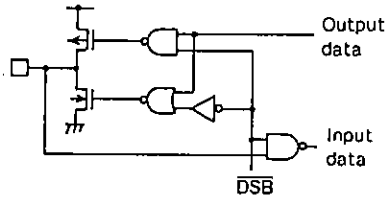
Option name	Selectable oscillation circuit	Condition
1. External clock source		- Schmitt trigger input
2. 2-pin (OSC1 and OSC2) RC oscillation circuit		- Schmitt trigger input
3. Ceramic resonator oscillation circuit		

(3) Option for selecting watchdog timer function

This option permits the user to select the watchdog timer function. This function could be helpful in detecting a timeout error from your user application program.

(4) Option for specifying port output type

i) This option permits the user to select a desired port output type of the following ports from the two output types listed in the table below. Please note that port output types can be specified in bit units.
Ports: P0, P1, P2, P3 (P33/$\overline{\text{HOLD}}$ not included), P4, P5, P6, and PC

Option name	Selected output circuit type	Conditions
1. Open drain output type		Ports P2, P3, P5 and P6 employ schmitt trigger input.
2. Pull-up transistor output type		Ports P2, P3, P5 and P6 employ schmitt trigger input. The Pch type MOS transistor can act as either a pull-up resistor (for Pu MOS output circuit) or an output transistor (CMOS output circuit), which depends on its driving capability. CMOS output type: P2, P3, P6, and PC. Pu MOS output: P0, P1, P4, P5.

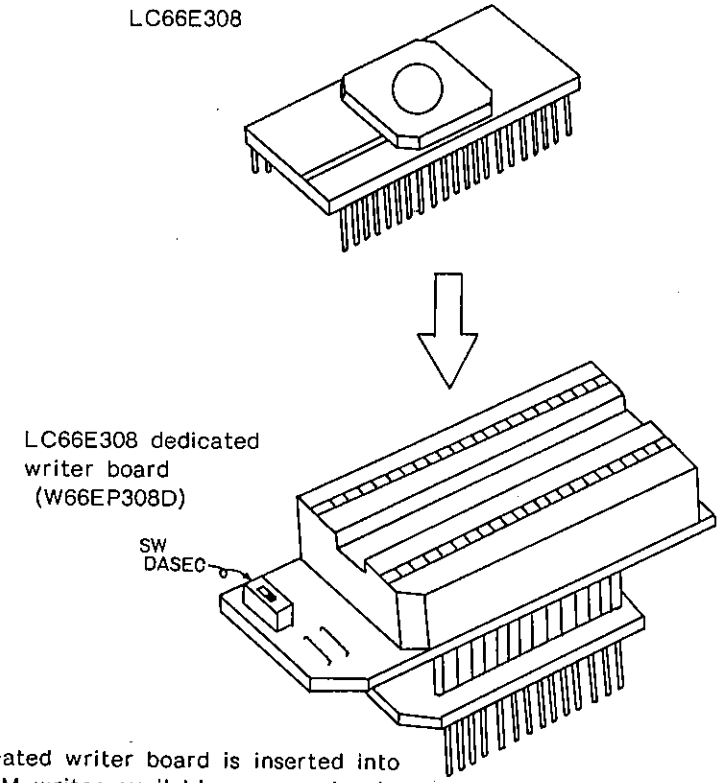
How to write data in the user option specification area and the program area in the on-chip EPROM

(1) Writing option codes to the user option specification area
Use the cross assembler "LC663S.EXE" when you write option codes in the user specification area and use the CPU pseudo instruction to set a Type No. to be evaluated and assemble your source application program. When your source application program is assembled, the option data will be stored in the user option specification area (2000 through 2007H). In addition to the above writing, you are allowed to write option data directly into the user option specification area in the on-chip EPROM. In this case, making references to the option code specification list on the next page will be a "must".

(2) Writing program into the on-chip EPROM program area
An EPROM writer available on your local market can be used to write program into the on-chip EPROM program area. In this case, the EPROM writer (27128 EPROM writer) must be used together with the dedicated writer board (W66EP308D) because the pin conversion (42 into 28) is required. The dedicated writer board is shown below.
The addresses should be set to 0000 to 2007H. If program is written mistakenly in 2008H onward, program may not be written/read normally.
Please note that the EPROM writer must be either an ADVANTEST product or the EVA850/800 accessory writer. Such an EPROM writer enables you to write your application program into the EPROM in Intel high-speed writing method.
When writing program, turn OFF switch DASEC on the writer board. If turned ON, program cannot be written/read normally.

(3) Using the data security function
When switch DASEC on the writer board is turned ON and the EPROM writer can be used for writing, the execution of the data security function is initiated and data output is brought to floating state thereafter (the error message appears on the EPROM writer, because the data security function is in operation. There is noting wrong with the LC66E308 or EPROM writer.) Erasing with ultraviolet ray makes it possible to write/read program again.

(4) How to erase the contents of the on-chip EPROM
To erase the contents of the on-chip EPROM, you can use an EPROM eraser available on your local market.



This dedicated writer board is inserted into the EPROM writer available on your local market. (select either an ADVANTEST writer product or the EVA850/800 accessory EPROM writer).

Option code specification list

ROM address	Bit	Optional item		Option data and selections
2000H	7 6 5	Unused		Always set to "0".
	4	Oscillation circuit type		1: Ceramic resonator oscillation. 0: RC oscillation or external clock source
	3	Unused		Always set to "0".
	2	P1	Output level at the system reset	1 = "H"-level 0 = "L"-level
	1	P0		
	0	Watchdog timer function option		1: Selected. 0: Not selected.
2001H	7	P13	Output circuit type	1 = PU, 0 = OD
	6	P12		
	5	P11		
	4	P10		
	3	P03	Output circuit type	1 = PU, 0 = OD
	2	P02		
	1	P01		
	0	P00		
2002H	7	Unused		Always set to "0".
	6	P32	Output circuit type	1 = PU, 0 = OD
	5	P31		
	4	P30		
	3	P23	Output circuit type	1 = PU, 0 = OD
	2	P22		
	1	P21		
	0	P20		
2003H	7	P53	Output circuit type	1 = PU, 0 = OD
	6	P52		
	5	P51		
	4	P50		
	3	P43	Output circuit type	1 = PU, 0 = OD
	2	P42		
	1	P41		
	0	P40		
2004H	7 6 5 4	Unused		Always set to "0".
	3	P63	Output circuit type	1 = PU, 0 = OD
	2	P62		
	1	P61		
	0	P60		
2005H	7 ~ 0	Unused		Always set to "0".
2006H	7 ~ 0	Unused		Always set to "0".
2007H	7 6 5 4	Unused		Always set to "0".
	3	PC3	Output circuit type	1 = PU, 0 = OD
	2	PC2		
	1 0	Unused		Always set to "0".

Remarks:

PU --- Pull-up MOS type resistance output

OD --- Open drain output

(1) Absolute maximum ratings (Ta = 25 °C and V_{SS} = 0V)

Characteristic	Symbol	Pins applicable and related information	Condition	Limits	Unit	Note
Supply voltage range	V_{DD} max	V_{DD}		−0.3~+7.0	V	
Input voltage range	V_{IN}(1)	P2, P3, (except P33/$\overline{HOLD}$), P4, P5 and P6.		−0.3~+15.0	V	1
	V_{IN}(2)	All the pins other than the above		−0.3~V_{DD}+0.3	V	2
Output voltage range	V_{OUT}(1)	P2, P3 (except P33/$\overline{HOLD}$), P4, P5 and P6.		−0.3~+15.0	V	1
	V_{OUT}(2)	All the pins other than the above.		−0.3~V_{DD}+0.3	V	2
Output current per pin	I_{ON}(1)	P0, P1, P2, P3 (except P33/$\overline{HOLD}$),P4, P5, P6 and PC.		20	mA	3
	−I_{OP}(1)	P0,P1,P4,P5,		2	mA	4
	−I_{OP}(2)	P2, P3 (except P33/$\overline{HOLD}$), P6 and PC.		4	mA	4
Pin total current	ΣI_{ON}(1)	P0, P1, P2, P3 (except P33/$\overline{HOLD}$), P40 and P41.		75	mA	3
	ΣI_{ON}(2)	P5, P6, P42, P43 and PC.		75	mA	3
	−ΣI_{OP}(1)	P0, P1, P2, P3 (except P33/$\overline{HOLD}$), P40 and P41.		25	mA	4
	−ΣI_{OP}(2)	P5, P6, P42, P43 and PC.		25	mA	4
Allowable power dissipation	Pd	Ta=+10~+40℃	DIC42S	600	mW	
Operating temperature range	Topr			+10~+40	℃	
Storage temperature range	Tstg			−55~+125	℃	

Note 1: Applicable only to the pins with open drain output circuit. Otherwise, refer to the values listed in the "all the pins other than the above" column.

Note 2: As far as oscillation input and output are concerned, the voltage range can cover the self-oscillating level.

Note 3: Sink current.

Note 4: Source current. Apply to the both of the pull-up output circuit and the CMOS output circuit.

(2) Allowable operating conditions (Ta = +10 ℃ to +40 ℃ and V_{SS} = 0V, unless otherwise noted)

Characteristic	Symbol	Pins applicable	Condition		Limits			Unit	Note
				V_{DD}(V)	min	typ	max		
Operating supply voltage range	V_{DD}	V_{DD}			4.5	5.0	5.5	V	
Memory backup voltage range	V_{DD}(H)	V_{DD}	With HOLD mode "ON"		1.8		5.5	V	
High level input voltage	V_{IH}(1)	P2,P3 (except P33/$\overline{HOLD}$),P4,P5 and P6.	With output Nch transistor "OFF"	4.5~5.5	0.75V_{DD}		+13.5	V	1
	V_{IH}(2)	P33/$\overline{HOLD}$, $\overline{RES}$, OSC1	With output Nch transistor "OFF"	4.5~5.5	0.75V_{DD}		V_{DD}	V	2
	V_{IH}(3)	P0, P1, PC, PD, PE	With output Nch transistor "OFF"	4.5~5.5	0.7V_{DD}		V_{DD}	V	3
	V_{IH}(4)	PE	With tri-state input mode selected	4.5~5.5	0.8V_{DD}		V_{DD}	V	

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Characteristic			Symbol	Pins applicable	Condition		Limits				Unit	Note
						V_{DD}(V)	min	typ	max			
Intermediate level input voltage range			V_{IM}	PE	With tri-state input mode selected.	4.5~5.5	0.4V_{DD}		0.6V_{DD}		V	
In-phase input voltage range			V_{CMM}	PD, PC2, PC3	With comparator input mode selected	4.5~5.5	1.0		V_{DD}−1.5		V	
Low level input voltage range			V_{IL}(1)	P2,P3 (except P33/$\overline{HOLD}$), P5,P6 and $\overline{RES}$, OSC1	With output Nch transistor "OFF"	4.5~5.5	V_{SS}		0.25V_{DD}		V	2
			V_{IL}(2)	P33/$\overline{HOLD}$		1.8~5.5	V_{SS}		0.25V_{DD}		V	
			V_{IL}(3)	P0, P1, P4, PC, PD, PE, TEST	With output Nch transistor "OFF"	4.5~5.5	V_{SS}		0.3V_{DD}		V	3
			V_{IL}(4)	PE	With tri-state input mode selected.	4.5~5.5	V_{SS}		0.2V_{DD}		.V	
Operating frequency (instruction cycle time)			f_{OP} (T_{CYC})			4.5~5.5	0.4 (10)		4.35 (0.92)		MHz (μs)	
External clock input mode	Frequency		f_{ext}	OSC1	Please refer to Figure 1. As it shows, input clocks reach the OSC1 pin from an external clock source and the OSC2 pin should be left open. The oscillation circuit option should be "external clock input".	4.5~5.5	0.4		4.35		MHz	
	Pulse width		t_{extH} t_{extL}		Please refer to Figure 1. As it shows, input clocks reach the OSC1 pin from an external clock source and the OSC2 pin should be left open. The oscillation circuit option should be "external clock input".	4.5~5.5	70				ns	
	Rise and Fall times		t_{extR} t_{extF}		Please refer to Figure 1. As it shows, input clocks reach the OSC1 pin from an external clock source and the OSC2 pin should be left open. The oscillation circuit option should be "external clock input".	4.5~5.5			30		ns	
Self oscillation mode	Ceramic resonator oscillation	Oscillation frequency	f_{CF}	OSC1, OSC2	Refer to Figure 2.	4MHz 4.5~5.5		4.0			MHz	
		Oscillation stabilization time period	t_{CFS}		Refer to Figure 3.	4MHz 4.5~5.5			10		ms	
	External R and C constants		Cext Rext	OSC1, OSC2	Refer to Figure 4.	4.5~5.5		100 TBD			pF kΩ	

Note 1: These values apply to the case where the open drain circuit type has been specified. Note that the P33/$\overline{HOLD}$ pin is not included (refer to the values listed in V_{IH} (2) column and that the pins P2, P3 and P6 cannot be used as the input pins as far as the CMOS output circuit type has been employed.

Note 2: These values apply to the case where the open drain circuit type has been selected.

Note 3: When the pin PE has been selected as the tri-state input pin, the values listed in the V_{IH}(4), V_{IM} and V_{IL}(4) columns should apply to the pin. Note that the pin PC cannot be used as the input pin as far as the CMOS type output circuit has been employed.

(3) Electrical characteristics (Ta = +10 °C to +40 °C and V_{SS} = 0V, unless otherwise noted)

Characteristic	Symbol	Pins applicable	Condition	V_{DD}(V)	Limits min	Limits typ	Limits max	Unit	Note
High level input current	$I_{IH}(1)$	P2,P3 (except P33/$\overline{HOLD}$), P4, P5 and P6.	V_{IN}=13.5V With output Nch transistor "OFF"	4.5~5.5			5.0	μA	1
	$I_{IH}(2)$	P0,P1,OSC1,$\overline{RES}$ and P33/$\overline{HOLD}$).	V_{IN}=V_{DD} With output Nch transistor "OFF"	4.5~5.5			1.0	μA	1
	$I_{IH}(3)$	PD, PE, PC2, PC3	V_{IN}=V_{DD} With output Nch transistor "OFF"	4.5~5.5			1.0	μA	1
Low level input current	$I_{IL}(1)$	Input pins other than PD, PE, PC2 and PC3	V_{IN}=V_{SS} With output Nch transistor "OFF"	4.5~5.5	−1.0			μA	2
	$I_{IL}(2)$	PC2, PC3, PD, PE	V_{IN}=V_{SS} With output Nch transistor "OFF"	4.5~5.5	−1.0			μA	2
High level output voltage	$V_{OH}(1)$	P2,P3 (except P33/$\overline{HOLD}$), P6 and PC.	I_{OH}=−1 mA	4.5~5.5	V_{DD}−1.0			V	3
			I_{OH}=−0.1mA	4.5~5.5	V_{DD}−0.5			V	3
	$V_{OH}(2)$	P0, P1, P4, P5	I_{OH}=−200μA	4.5	2.4			V	4
			I_{OH}=−130μA	4.5~5.5	V_{DD}−1.35			V	4
Output pull-up current	I_{PO}	P0, P1, P4, P5	V_{IN}=V_{SS}	5.5	−1.6			mA	4
Low level output voltage	$V_{OL}(1)$	P0,P1,P2,P3 (except P33/$\overline{HOLD}$), P4,P5, P6 and PC.	I_{OL}=1.6mA	4.5~5.5			0.4	V	
	$V_{OL}(2)$	P0,P1,P2,P3 (except P33/$\overline{HOLD}$), P4,P5, P6 and PC.	I_{OL}=10mA	4.5~5.5			1.5	V	
Output-OFF leakage current	$I_{OFF}(1)$	P2,P3,P4,P5,P6	V_{IN}=13.5V	4.5~5.5			5.0	μA	5
	$I_{OFF}(2)$	P0, P1, PC	V_{IN}=V_{DD}	4.5~5.5			1.0	μA	5
Comparator offset current	V_{OFF}	PD	V_{IN}=1.0V ~V_{DD}−1.5V	4.5~5.5		±50	±300	mV	
Schmitt characteristics: Hysteresis voltage	V_{HYS}	P2, P3, P5, P6, $\overline{RES}$, OSC1 (RC, EXT)		4.5~5.5		0.1V_{DD}		V	
Schmitt characteristics: High level threshold voltage	Vt H				0.5V_{DD}		0.75V_{DD}	V	
Schmitt characteristics: Low level threshold voltage	Vt L				0.25V_{DD}		0.5V_{DD}	V	
RC oscillation frequency range	f_{RC}	OSC1, OSC2	Refer to Figure 4. C=100pF± 5 % R=TBD	4.5~5.5	T.B.D	3.0	T.B.D	MHz	

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Characteristic			Symbol	Pins applicable		Condition		Limits			Unit	Note
							VDD(V)	min	typ	max		
Serial timing clock	Cycle time	Data input	tCKCY	$\overline{SCK0}$, $\overline{SCK1}$		Refer to Figure 5 (timings) and Figure 6 (test load)	4.5~5.5	0.9			μs	
		Data output					4.5~5.5	2.0			TCYC	
	Low level and High level pulse width	Data input	tCKL				4.5~5.5	0.4			μs	
		Data output	tCKH				4.5~5.5	1.0			TCYC	
	Rise and Fall time	Data output	tCKR tCKF				4.5~5.5			0.1	μs	
Serial input	Data setup time		tICK	SI0, SI1		Refer to Figure 5 (timings). Time periods based on the $\overline{SCK0}$ and $\overline{SCK1}$ clock rising edges.	4.5~5.5	0.3			μs	
	Data HOLD time		tCKI				4.5~5.5	0.3			μs	
Serial output	Output delay time		tCKO	SO0, SO1		Refer to Figure 5 (timings) and Figure 6 (test load). Time period based on the $\overline{SCK0}$ and $\overline{SCK1}$ clock falling edges.	4.5~5.5			0.3	μs	
Pulse input condition	INT0 High level and Low level pulse width		tI0H tI0L	INT0	Refer to Figure 7.	- With INT0 interrupt request input acceptable. - With event counter (timer 0) input or pulse width measuring input acceptable.	4.5~5.5	2			TCYC	
	High level and Low level pulse width (INT0 not included)		tI1H tI1L	$\overline{INT1}$, $\overline{INT2}$		- With interrupt request inputs acceptable		2			TCYC	
	PIN1 High level and Low level pulse width		tPINH tPINL	PIN1		- With event counter (timer 1) input acceptable		2			TCYC	
	$\overline{RES}$ High level and Low level pulse width		tRSH tRSL	$\overline{RES}$		- With reset request acceptable		3			TCYC	
Comparator response speed			TRS	PD	Refer to Figure 8.		4.5~5.5			30	μs	
Current dissipation during basis operation mode			IDD OP	VDD		4 MHz ceramic oscillation	4.5~5.5		4.5	8	mA	
						4 MHz external clock source			6.5	11	mA	6
						RC oscillation			4.0	8	mA	

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Characteristic	Symbol	Pin applicable	Condition	Limits				Unit	Note
				V_{DD}(V)	min	typ	max		
Current dissipation during HALT operation mode	I_{DDHALT}	V_{DD}	4 MHz ceramic resonator oscillation	4.5~5.5		3	5	mA	
			4 MHz external clock source			3.5	6	mA	
			RC oscillation			3	5	mA	
Current dissipation during HOLD operation mode	I_{DDHOLD}	V_{DD}		1.8~5.5		0.01	10	μA	

Note 1: Applicable to the case where input/output common ports have been set to open drain output circuit type and the output Nch transistors have been in OFF state. Note that the input/output common ports cannot be used as the input port if they have been set to the CMOS output circuit type.

Note 2: Applicable to the case where input/output common ports have been set to open drain output circuit type and the output Nch transistors have been in OFF state. If the pull-up transistor output circuit type has been employed, please refer to the value listed in the output pull-up current column (IPO). Note that input/output common ports cannot be used as the input ports if they have been set to the CMOS output circuit type.

Note 3: Applicable to the case where the ports have been set to the CMOS output circuit type and the output Nch transistors have been in OFF state.

Note 4: Applicable to the case where the ports have been set to the pull-up resistor output circuit type and the output Nch transistors have been in OFF state.

Note 5: Applicable to the case where the ports have been set to the open drain output circuit type and the output Nch transistors have been in OFF state.

Note 6: Reset mode.

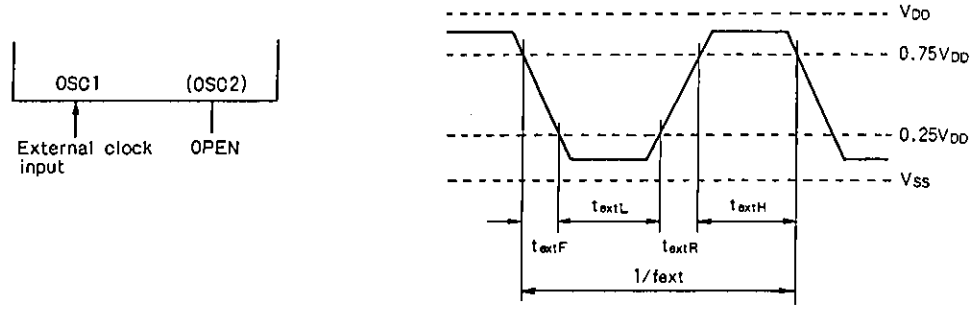


Figure 1. External clock input waveform

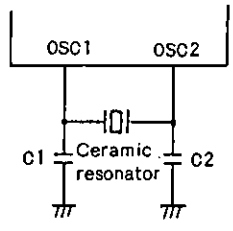


Figure 2. Ceramic resonator oscillation circuit

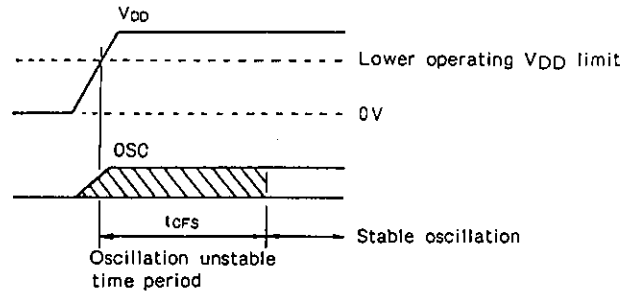


Figure 3. Oscillation stabilization time

Capacitance (external)	4 MHz (Murata) CSA4.00MG	C1	33pF ±10%
		C2	33pF ±10%
	4 MHz (Kyocera) KBR4.0MS	C1	33pF ±10%
		C2	33pF ±10%
Capacitance (internal)	4 MHz (Murata) CST4.00MG		
	4 MHz (Kyocera) KBR-4.0MES		

Table 1. Ceramic resonator oscillation constants (recommended)

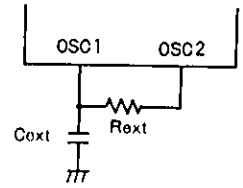


Figure 4. RC oscillation

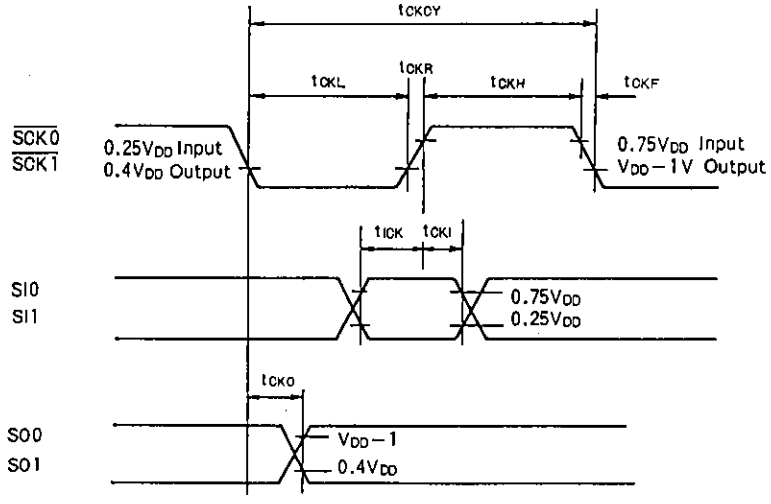


Figure 5. Serial input/output timings

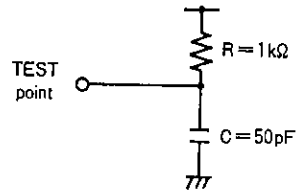


Figure 6. Timing load

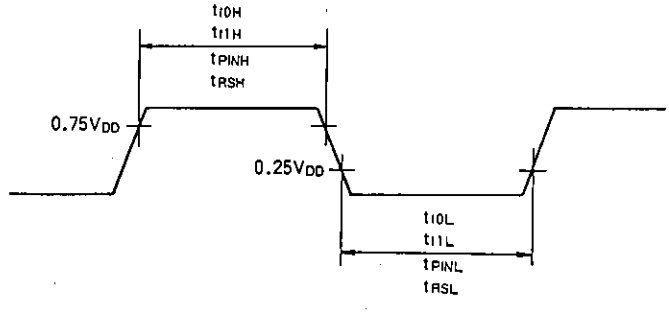


Figure 7. Input timings for INT0, $\overline{INT1}$, $\overline{INT2}$, PIN1 and $\overline{RES}$

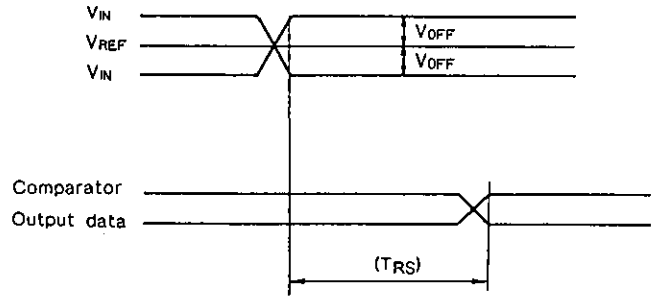


Figure 8. Comparator response speed (T_{RS}) and output timing

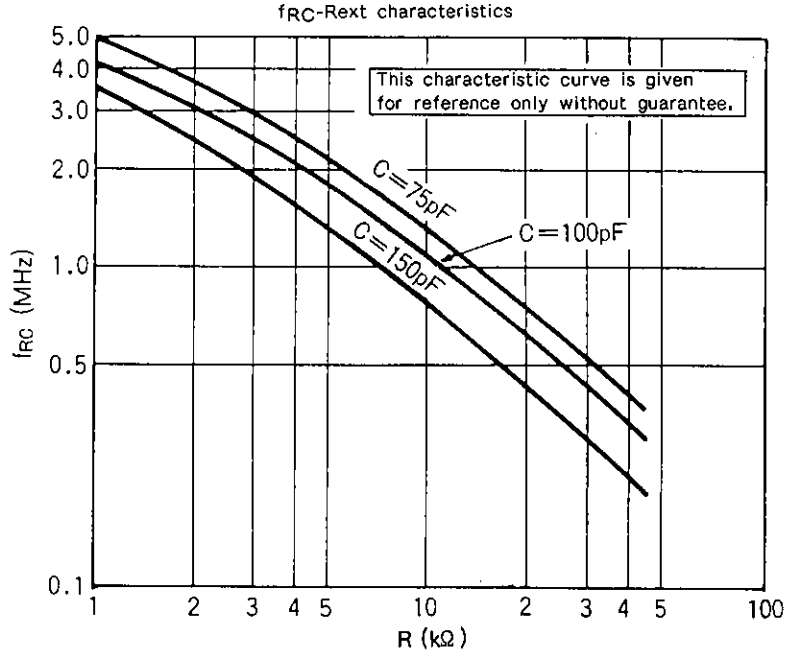
LC66E308 RC oscillation characteristics

Figure 9 shows the RC oscillation characteristics of the LC66E308 microcomputer.
The RC oscillation frequency range that can be guaranteed is shown below with the external constants and other conditions:

$$T.B.D \leqq f_{RC} \leqq T.B.D$$

External constants --- Cext = 100pF and Rext = TBD
Ta = +10 °C to +40 °C and V_{DD} = 4.5V to 5.5V

If you are to employ the external constants other than the above, the Rext and the Cext should be within the range between T.B.D kΩ and T.B.D kΩ, and between T.B.D pF and T.B.D pF, respectively. Please take a close look at the figure below.
Note 10: With V_{DD} = 4.5V to 5.5V and Ta = +10°C to +40°C, the oscillation frequency to be selected should meet the requirement that the operating frequencies in the range between 0.4MHz and 4.3MHz must be provided without fail.



These values shown here are not guarantees nor recommendations. Instead, they are referencing values. It is well understood among designers that these values are strongly dependent on the application and its requirements. In any case, their suitability should be verified by environment testing before the design is submitted to production.

Figure 9. RC oscillation frequency reference values

LC6630X SERIES INSTRUCTION SET (BY FUNCTION)

Symbol	Description
AC	: Accumulator
E	: E register
CF	: Carry flag
ZF	: Zero flag
HL	: Data pointer DPH, DPL
XY	: Data pointer DPX, DPY
M	: Data memory
M (HL)	: Data memory contents specified by data pointer DPH, DPL
M (XY)	: Data memory contents specified by supplementary data pointer DPX, DPY
M2 (HL)	: 2-word data memory contents specified by data pointer DPH, DPL. In this case, the accessed data memory area address must be multiples of 2 (even address).
SP	: Stack pointer
M2 (SP)	: 2-word data memory contents specified by stack pointer
M4 (SP)	: 4-word data memory contents specified by stack pointer
in	: n-bit immediate data
t2	: Bit specification

t2	11	10	01	00
Bit	2^3	2^2	2^1	2^0

PCh	: Bits 8 to 11 of PC
PCm	: Bits 4 to 7 of PC
PCl	: Bits 0 to 3 of PC
Fn	: User's flag n=0 to 15
TIMER0	: Timer 0
TIMER1	: Timer 1
SIO	: Serial register
P	: Port
P (i4)	: Port contents specified by 4-bit immediate data
INT	: Interrupt enable flag
( ),[ ]	: Contents
←	: Transfer direction and operation result
∀	: Exclusive logical sum
∧	: Logical product
∨	: Logical sum
+	: Addition
−	: Subtraction
—	: 1's complement

Instruction type	Mnemonics		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 0 0 0	0 0 0 0	1	1	AC←0 (Equivalent to LAI 0)	Clears AC.	ZF	Only the first instruction is effective if executed continuously (skip function).
	DAA	Decimal adjust AC in addition	1 1 0 0 0 0 1 0	1 1 1 1 0 1 1 0	2	2	AC←(AC)+6 (Equivalent to ADI 6)	Adds 6 to AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 0 0 0 0 1 0	1 1 1 1 1 0 1 0	2	2	AC←(AC)+10 (Equivalent to ADI 0AH)	Adds 10 to AC.	ZF	
	CLC	Clear CF	0 0 0 1	1 1 1 0	1	1	CF←0	Clears CF.	CF	
	STC	Set CF	0 0 0 1	1 1 1 1	1	1	CF←1	Sets CF.	CF	
	CMA	Complement AC	0 0 0 1	1 0 0 0	1	1	AC←$\overline{(AC)}$	Gives 1's complement of (invert) AC.	ZF	
	IA	Increment AC	0 0 0 1	0 1 0 0	1	1	AC←(AC)+1	Adds a to AC.	ZF, CF	
	DA	Decrement AC	0 0 1 0	0 1 0 0	1	1	AC←(AC)−1	Subtracts 1 from AC.	ZF, CF	
	RAR	Rotate AC right through CF	0 0 0 1	0 0 0 0	1	1	AC_3←(CF), ACn←(ACn+1), CF←(AC_0)	Rotates AC right through CF.	CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0←(CF), ACn+1←(ACn), CF←(AC_3)	Rotates AC left through CF.	CF, ZF	
	TAE	Transfer AC to E	0 1 0 0	0 1 0 1	1	1	E←(AC)	Transfers the AC contents to the E register.		
	TEA	Transfer E to AC	0 1 0 0	0 1 1 0	1	1	AC←(E)	Transfers the E register contents to AC.	ZF	
	XAE	Exchange AC with E	0 1 0 0	0 1 0 0	1	1	(AC)↔(E)	Exchanges the contents of the AC and E register.		
Memory manipulation instructions	IM	Increment M	0 0 0 1	0 0 1 0	1	1	M(HL)←(M(HL))+1	Adds 1 to M(HL).	ZF, CF	
	DM	Decrement M	0 0 1 0	0 0 1 0	1	1	M(HL)←(M(HL))−1	Subtracts 1 from M(HL).	ZF, CF	
	IMDR i8	Increment M direct	1 1 0 0 I_7 I_6 I_5 I_4	0 1 1 1 I_3 I_2 I_1 I_0	2	2	M(i8)←(M(i8))+1	Adds 1 to M(i8).	ZF, CF	
	DMDR i8	Decrement M direct	1 1 0 0 I_7 I_6 I_5 I_4	0 0 1 1 I_3 I_2 I_1 I_0	2	2	M(i8)←(M(i8))−1	Subtracts 1 from M(i8).	ZF, CF	
	SMB t2	Set M data bit	0 0 0 0	1 1 t_1 t_0	1	1	(M(HL), t2)←1	Sets a bit specified by t1t0 of M(HL).		
	RMB t2	Reset M data bit	0 0 1 0	1 1 t_1 t_0	1	1	(M(HL), t2)←0	Resets a bit specified by t1t0 of M(HL).	ZF	
Operation/Comparison instructions	AD	Add M to AC	0 0 0 0	0 1 1 0	1	1	AC←(AC)+(M(HL))	Adds together the contents of AC and M(HL) in binary and stores the result in AC.	ZF, CF	
	ADDR i8	Add M direct to AC	1 1 0 0 I_7 I_6 I_5 I_4	1 0 0 1 I_3 I_2 I_1 I_0	2	2	AC←(AC)+(M(i8))	Adds together the contents of AC and M(i8) in binary and stores the result in AC.	ZF, CF	
	ADC	Add M to AC with CF	0 0 0 0	0 0 1 0	1	1	AC←(AC)+(M(HL))+(CF)	Adds together the contents of AC, M(HL), and CF in binary and stores the result in AC.	ZF, CF	
	ADI i4	Add immediate data to AC	1 1 0 0 0 0 1 0	1 1 1 1 I_3 I_2 I_1 I_0	2	2	AC←(AC)+I_3,I_2,I_1,I_0	Adds together the contents of AC and immediate data in binary and stores the result in AC.	ZF	
	SUBC	Subtract AC from M with CF	0 0 0 1	0 1 1 1	1	1	AC←(M(HL))−(AC)−($\overline{CF}$)	Subtracts the contents of AC from M(HL) with $\overline{CF}$ in binary and stores the result in AC.	ZF, CF	CF=0 if there is a borrow while CF=1 if there is no borrow.
	ANDA	AND M with AC then store AC	0 0 0 0	0 1 1 1	1	1	AC←(AC)∧(M(HL))	Performs a logical AND operation between AC and M(HL) and stores the result in AC.	ZF	
	ORA	OR M with AC then store AC	0 0 0 0	0 1 0 1	1	1	AC←(AC)∨(M(HL))	Performs a logical OR operation between AC and M(HL) and stores the result in AC.	ZF	
	EXL	Exclusive OR M with AC then store AC	0 0 0 1	0 1 0 1	1	1	AC←(AC)∀(M(HL))	Performs a logical exclusive OR operation between AC and M(HL) and stores the result in AC.	ZF	
	ANDM	AND M with AC then store M	0 0 0 0	0 0 1 1	1	1	M(HL)←(AC)∧(M(HL))	Performs a logical AND operation between AC and M(HL) and stores the result in M(HL).	ZF	
	ORM	OR M with AC then store M	0 0 0 0	0 1 0 0	1	1	M(HL)←(AC)∨(M(HL))	Performs a logical OR operation between AC and M(HL) and stores the results in M(HL).	ZF	

Instruction type	Mnemonics		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Operation/Comparison instructions	CM	Compare AC with M	0 0 0 1	0 1 1 0	1	1	$\overline{(M(HL))}+(AC)+1$	Compares the contents of AC and M(HL) and then sets/resets the carry flag (CF) and zero flag (ZF). Comparison relations: (M(HL))>(AC): CF=0, ZF=0; (M(HL))=(AC): CF=1, ZF=1; (M(HL))<(AC): CF=1, ZF=0	ZF, CF	
	CI i4	Compare AC with immediate data	1 1 0 0 1 0 1 0	1 1 1 1 $I_3 I_2 I_1 I_0$	2	2	$\overline{I_3 I_2 I_1 I_0}+(AC)+1$	Compares the contents of the accumulator (AC) and immediate data I3I2I1I0 and sets/resets the zero flag (ZF) and carry flag (CF). Comparison relations: $I_3 I_2 I_1 I_0$>AC: CF=0, ZF=0; $I_3 I_2 I_1 I_0$=AC: CF=1, ZF=1; $I_3 I_2 I_1 I_0$<AC: CF=1, ZF=0	ZF, CF	
	CLI i4	Compare DP_L with immediate data	1 1 0 0 1 0 1 1	1 1 1 1 $I_3 I_2 I_1 I_0$	2	2	ZF←1 if(DP_L)=$I_3 I_2 I_1 I_0$ ZF←0 if(DP_L)≠$I_3 I_2 I_1 I_0$	Compares the contents of DP_L and immediate data and sets the zero flag (ZF) if they are equal, or resets the flag if not equal.	ZF	
	CMB t2	Compare AC bit with M data bit	1 1 0 0 1 1 0 1	1 1 1 1 0 0 t_1 t_0	2	2	ZF←1 if(AC, t2)=(M(HL), t2) ZF←0 if(AC, t2)≠(M(HL), t2)	Compares the contents of AC and M(HL) bit specified by the 2 bits (t1 and t2) of the instruction and sets the zero flag (ZF) if they are equal, or resets the flag if not equal.	ZF	
Load/store instructions	LAE	Load AC and E from M2 (HL)	0 1 0 1	1 1 0 0	1	1	AC←M(HL) E←M(HL+1)	Loads the contents of M2(HL) into the AC and the E register.		
	LAI i4	Load AC with immediate data	1 0 0 0	$I_3 I_2 I_1 I_0$	1	1	AC←$I_3 I_2 I_1 I_0$	Loads immediate data into AC.	ZF	Only the first instruction is effective if executed continuously (skip function)
	LADR i8	Load AC from M direct	1 1 0 0 $I_7 I_6 I_5 I_4$	0 0 0 1 $I_3 I_2 I_1 I_0$	2	2	AC←(M(i8))	Loads the contents of M(i8) into AC.	ZF	
	S	Store AC to M	0 1 0 0	0 1 1 1	1	1	M(HL)←(AC)	Stores the contents of AC into M(HL).		
	SAE	Store AC and E to M2 (HL)	0 1 0 1	1 1 1 0	1	1	M(HL)←(AC) M(HL+1)←(E)	Stores the contents of AC and the E register into M2(HL).		
	LA reg	Load AC from M(reg)	0 1 0 0	1 0 t_0 0	1	1	AC←(M(reg))	Loads the contents of M(reg) into AC. reg is either an HL or XY. reg: HL → t_0=0; XY → t_0=1	ZF	
	LA reg,I	Load AC from M(reg) then increment reg	0 1 0 0	1 0 t_0 1	1	2	AC←(M(reg)) DP_L←(DP_L)+1 or DP_Y←(DP_Y)+1	Loads the contents of M(reg) into the accumulator (AC). reg is either an HL or XY. After loading, increments the contents of DP_L or DPY. Refer to the LA reg instruction for the relationship between reg and t0.	ZF	ZF status depends on DP_L or DPY increment result.
	LA reg, D	Load AC from M(reg) then decrement reg	0 1 0 1	1 0 t_0 1	1	2	AC←(M(reg)) DP_L←(DP_L)−1 or DP_Y←(DP_Y)−1	Loads the contents of M(reg) into AC. reg is either an HL or XY. After loading, decrements the contents of DP_L or DPY. Refer to the LA reg instruction for the relationship between reg and t0.	ZF	ZF status depends on DP_L or DPY decrement result.
	XA reg	Exchange AC with M (reg)	0 1 0 0	1 1 t_0 0	1	1	(AC)↔(M(reg))	Exchanges the contents of AC and M(reg). reg is either an HL or XY. reg: HL → t_0=0; XY → t_0=1		
	XA reg,I	Exchange AC with M (reg) then increment reg	0 1 0 0	1 1 t_0 1	1	2	(AC)↔(M(reg)) DP_L←(DP_L)+1 or DP_Y←(DP_Y)+1	Exchanges the contents of AC and M(reg). reg is either an HL or XY. After exchanging, increments the contents of DP_L or DPY. Refer to the XA reg instruction for the relationship between reg and t0.	ZF	ZF status depends on DP_L or DPY increment result.
	XA reg, D	Exchange AC with M (reg) then decrement reg	0 1 0 1	1 1 t_0 1	1	2	(AC)↔(M(reg)) DP_L←(DP_L)−1 or DP_Y←(DP_Y)−1	Exchanges the contents of AC and M(reg). reg is either an HL or XY. After exchanging, decrements the contents of DP_L or DPY. Refer to the XA reg instruction for the relationship between reg and t0.	ZF	ZF status depends on DP_L or DPY decrement result.
	XADR i8	Exchange AC with M direct	1 1 0 0 $I_7 I_6 I_5 I_4$	1 0 0 0 $I_3 I_2 I_1 I_0$	2	2	(AC)↔(M(i8))	Exchanges the contents of AC and M(i8).		

Instruction type	Mnemonics		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Load/store instructions	LEAI i8	Load E & AC with immediate data	1 1 0 0 I_7 I_6 I_5 I_4	0 1 1 0 I_3 I_2 I_1 I_0	2	2	E ← I_7 I_6 I_5 I_4 AC ← I_3 I_2 I_1 I_0	Loads immediate data i8 into the E register and the accumulator (AC).		
	RTBL	Read table data from program ROM	0 1 0 1	1 0 1 0	1	2	E, AC ← (ROM(PCh, E, AC))	First, replace the contents of lower 8 bits of PC with the E register and AC contents. Then, loads the ROM data at an address specified by the new contents of the lower 8 bits of PC into the E register and AC.		
	RTBLP	Read table data from program ROM then output to P4, 5	0 1 0 1	1 0 0 0	1	2	Port 4, 5 ← (ROM(PCh, E, AC))	First, replaces the contents of lower 8 bits of AC with the E register and AC contents. Then, outputs the ROM data at an address specified by the new contents of the lower 8 bits of PC to ports 4 and 5.		
Data pointer manipulation instructions	LDZ i4	Load DP_H with zero and DP_L with immediate data respectively	0 1 1 0	I_3 I_2 I_1 I_0	1	1	DP_H ← 0 DP_L ← I_3 I_2 I_1 I_0	Loads the data of 0 (zero) and immediate data i4 into the DP_H and DP_L respecitively.		
	LHI i4	Load DP_H with immediate data	1 1 0 0 0 0 0 0	1 1 1 1 I_3 I_2 I_1 I_0	2	2	DP_H ← I_3 I_2 I_1 I_0	Loads immediate data i4 into the DP_H.		
	LLI i4	Load DP_L with immediate data	1 1 0 0 0 0 0 1	1 1 1 1 I_3 I_2 I_1 I_0	2	2	DP_L ← I_3 I_2 I_1 I_0	Loads immediate data i4 into the DP_L.		
	LHLI i8	Load DP_H, DP_L with immediate data	1 1 0 0 I_7 I_6 I_5 I_4	0 0 0 0 I_3 I_2 I_1 I_0	2	2	DP_H ← I_7 I_6 I_5 I_4 DP_L ← I_3 I_2 I_1 I_0	Loads immediate data into the DP_H and DP_L.		
	LXYI i8	Load DP_X, DP_Y with immediate data	1 1 0 0 I_7 I_6 I_5 I_4	0 0 1 0 I_3 I_2 I_1 I_0	2	2	DP_X ← I_7 I_6 I_5 I_4 DP_Y ← I_3 I_2 I_1 I_0	Loads immediate data into the DP_X and DP_Y.		
	IL	Increment DP_L	0 0 0 1	0 0 0 1	1	1	DP_L ← (DP_L) + 1	Increments the contents of the DP_L by 1.	ZF	
	DL	Decrement DP_L	0 0 1 0	0 0 0 1	1	1	DP_L ← (DP_L) − 1	Decrements the contents of the DP_L by 1.	ZF	
	IY	Increment DP_Y	0 0 0 1	0 0 1 1	1	1	DP_Y ← (DP_Y) + 1	Increments the contents of the DP_Y by 1.	ZF	
	DY	Decrement DP_Y	0 0 1 0	0 0 1 1	1	1	DP_Y ← (DP_Y) − 1	Decrements the contents of the DP_Y by 1.	ZF	
	TAH	Transfer AC to DP_H	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 0	2	2	DP_H ← (AC)	Transfers the contents of the accumulator (AC) to the DP_H.		
	THA	Transfer DP_H to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 0	2	2	AC ← (DP_H)	Transfers the contents of the DP_H to the AC.	ZF	
	XAH	Exchange AC with DP_H	0 1 0 0	0 0 0 0	1	1	(AC) ↔ (DP_H)	Exchanges the contents of the accumulator (AC) and the DP_H.		
	TAL	Transfer AC to DP_L	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 1	2	2	DP_L ← (AC)	Transfers the contents of the accumulator (AC) to the DP_L.		
	TLA	Transfer DP_L to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 1	2	2	AC ← (DP_L)	Transfers the contents of the DP_L to the accumulator (AC).	ZF	
	XAL	Exchange AC with DP_L	0 1 0 0	0 0 0 1	1	1	(AC) ↔ (DP_L)	Exchanges the contents of the AC and DP_L.		
	TAX	Transfer AC to DP_X	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 0	2	2	DP_X ← (AC)	Transfers the contents of the accumulator (AC) to the DP_X.		
	TXA	Transfer DP_X to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 0	2	2	AC ← (DP_X)	Transfers the contents of DP_X to the AC.	ZF	
	XAX	Exchange AC with DP_X	0 1 0 0	0 0 1 0	1	1	(AC) ↔ (DP_X)	Exchanges the contents of the AC and DP_X.		
	TAY	Transfer AC to DP_Y	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 1	2	2	DP_Y ← (AC)	Transfers the contents of the accumulator (AC) to the DP_Y.		
	TYA	Transfer DP_Y to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 1	2	2	AC ← (DP_Y)	Transfers the contents of the DP_Y to the AC.	ZF	
	XAY	Exchange AC with DP_Y	0 1 0 0	0 0 1 1	1	1	(AC) ↔ (DP_Y)	Exchanges the contents of the accumulator (AC) and the DP_Y.		
Flag manipulation instructions	SFB n4	Set flag bit	0 1 1 1	$n_3n_2n_1n_0$	1	1	Fn ← 1	Sets a flag specified by n4.		
	RFB n4	Reset flag bit	0 0 1 1	$n_3n_2n_1n_0$	1	1	Fn ← 0	Resets a flag specified by n4.	ZF	
Jump/subroutine instructions	JMP addr	Jump in the current bank	1 1 1 0 $P_7P_6P_5P_4$	$P_{11}P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	PC12 ← PC12 PC11~0 ← P_{11} ~ P_0	Jumps to an address specified by immediate data P_{11} ~ P_0 in the current bank.		When executed immediately after the BANK instruction, PC12 ← (PC12).
	JPEA	Jump to the address stored at E and AC in the current page	0 0 1 0	0 1 1 1	1	1	PC12~PC8 ← PC12~PC8 PC7~4 ← (E) PC3~0 ← (AC)	Jumps to an address specified by the contents of the E register and accumulator (AC) which have replaced the contents of lower 8 bits of the program counter (PC).		

Instruction type	Mnemonics		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Jump/subroutine instructions	CAL addr	Call subroutine	0 1 0 1 $P_7P_6P_5P_4$	0 $P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	PC12-11←0 PC10~0←P_{10}~P_0 M4(SP)←(CF, ZF, PC12~0) SP←(SP)-4	Calls a subroutine.		
	CZP addr	Call sudroutine in the zero page	1 0 1 0	$P_3P_2P_1P_0$	1	2	PC12~6, PC1~0←0 PC5~2←P_3~P_0 M4(SP)←(CF, ZF, PC12~0) SP←SP-4	Calls a subroutine in page 0 of bank 0.		
	BANK	Change bank	0 0 0 1	1 0 1 1	1	1		Changes memory banks and register banks.		
	PUSH reg	Push reg on M2(SP)	1 1 0 0 1 1 1 1	1 1 1 1 1 i_1 i_0 0	2	2	M2(SP)←(reg) SP←(SP)-2	Stores the contents of reg into the M2(SP) and then subtracts 2 from the stack pointer (SP). reg: HL (i_1 i_0 = 0 0); XY (0 1); AE (1 0); Inhibited (1 1)		
	POP reg	Pop reg off M2(SP)	1 1 0 0 1 1 1 0	1 1 1 1 1 i_1 i_0 0	2	2	SP←(SP)+2 reg←(M2(SP))	Stores the contents of reg into the M2(SP) and then increments the contents of the stack pointer (SP) by 2 and loads the contents of M2 (SP) into a reg. Refer to the PUSH reg instruction for the relationship between i1i0 and reg.		
	RT	Return from subroutine	0 0 0 1	1 1 0 0	1	2	SP←(SP)+4 PC←(M4(SP))	Returns execution from a subroutine or interrupt processing routine back to the routine that called it. The contents of the carry flag (CF) and zero flag (ZF) are not returned from the stack area.		
	RTI	Return from interrupt routine	0 0 0 1	1 1 0 1	1	2	SP←(SP)+4 PC←(M4(SP)) CF, ZF←(M4(SP))	Returns execution from a subroutine or interrupt processing routine back to the routine that called it. The contents of the carry flag (CF) and zero flag (ZF) are returned from the stack area.	ZF, CF	
Branch instructions	BAt2 addr	Branch on AC bit	1 1 0 1 $P_7P_6P_5P_4$	0 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(AC, t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of AC is 1 (program branch).		
	BNAt2 addr	Branch on no AC bit	1 0 0 1 $P_7P_6P_5P_4$	0 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(AC, t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of AC is 0 (program branch).		
	BMt2 addr	Branch on M bit	1 1 0 1 $P_7P_6P_5P_4$	0 1 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(M(HL), t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of M(HL) is 1 (program branch).		
	BNMt2 addr	Branch on no M bit	1 0 0 1 $P_7P_6P_5P_4$	0 1 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(M(HL), t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of M(HL) is 0 (program branch).		
	BPt2 addr	Branch on Port bit	1 1 0 1 $P_7P_6P_5P_4$	1 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(P(DPL), t2)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of the port accessed by DPL is 1 (program branch).		Used to manipulate internal control registers if executed immediately after the BANK instruction. In this case, the internal control registers must be readable.
	BNPt2 addr	Branch on no Port bit	1 0 0 1 $P_7P_6P_5P_4$	1 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(P(DPL), t2)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if a bit specified by immediate data t1t0 of the port accessed by DPL is 0 (program branch).		Same as above.
	BC addr	Branch on CF	1 1 0 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(CF)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the carry flag (CF) is 1 (program branch).		
	BNC addr	Branch on no CF	1 0 0 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(CF)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the carry flag (CF) is 0 (program branch).		
	BZ addr	Branch on ZF	1 1 0 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(ZF)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the zero flag (ZF) is 1 (program branch).		
	BNZ addr	Branch on no ZF	1 0 0 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(ZF)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the zero flag (ZF) is 0 (program branch).		

Instruction type	Mnemonics		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Branch instructions	BFn4 addr	Branch on flag bit	1 1 1 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(Fn)=1	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the flag specified by n3n2n1n0 is 1. The flag is one of the 16 flags.		
	BNFn4 addr	Branch on no flag bit	1 0 1 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(Fn)=0	Transfers execution to an address specified by the contents of P7 to P0 in the current page if the content of the flag specified by n3n2n1n0 is 0. The flag is one of the 16 flags.		
Input/output instructions	IP0	Input port 0 to AC	0 0 1 0	0 0 0 0	1	1	AC←(P0)	Inputs the contents of port 0 to the accumulator (AC).	ZF	
	IP	Input port to AC	0 0 1 0	0 1 1 0	1	1	AC←(P(DP_L))	Inputs the contents of port accessed by DP_L to the accumulator (AC).	ZF	
	IPM	Input port to M	0 0 0 1	1 0 0 1	1	1	M(HL)←(P(DP_L))	Inputs the contents of port accessed by DP_L to the M(HL).		
	IPDR i4	Input port to AC direct	1 1 0 0 0 1 1 0	1 1 1 1 I_3 I_2 I_1 I_0	2	2	AC←(P(i4))	Inputs the contents of port accessed by i4 to the accumulator (AC).	ZF	
	IP45	Input port 4,5 to E, AC respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 0	2	2	E ←(P(4)) AC←(P(5))	Inputs the contents of ports 4 and 5 to the E register and accumulator (AC) respectively.		
	OP	Output AC to port	0 0 1 0	0 1 0 1	1	1	P(DP_L)←(AC)	Outputs the contents of the accumulator (AC) to a port accessed by DP_L.		
	OPM	Output M to port	0 0 0 1	1 0 1 0	1	1	P(DP_L)←(M(HL))	Outputs the contents of the M(HL) to a port accessed by DP_L.		
	OPDR i4	Output AC to port direct	1 1 0 0 0 1 1 1	1 1 1 1 I_3 I_2 I_1 I_0	2	2	P(i4)←(AC)	Outputs the contents of the accumulator (AC) to a port accessed by i4.		
	OP45	Output E, AC to port 4,5 respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 1	2	2	P(4)←(E) P(5)←(AC)	Outputs the contents of the E register and accumulator (AC) to ports 4 and 5 respectively.		
	SPB t2	Set port bit	0 0 0 0	1 0 t_1 t_0	1	1	(P(DP_L), t2)←1	Sets a bit specified by immediate data t1t0 of a port accessed by DP_L.		
	RPB t2	Reset port bit	0 0 1 0	1 0 t_1 t_0	1	1	(P(DP_L), t2)←0	Resets a bit specified by immediate data t1t0 of a port accessed by DP_L.	ZF	
	ANDPDR i4, p4	AND port with immediate data then output	1 1 0 0 I_3 I_2 I_1 I_0	0 1 0 1 $P_3P_2P_1P_0$	2	2	P(P_3~P_0)←(P(P_3~P_0))∨I_3~I_0	Performs a logical AND operation between the contents of a port specified by P3 to P0 and immediate data I3I2I1I0 and outputs the resulted product to the port.	ZF	
	ORPDR i4, p4	OR port with immediate data then output	1 1 0 0 I_3 I_2 I_1 I_0	0 1 0 0 $P_3P_2P_1P_0$	2	2	P(P_3~P_0)←(P(P_3~P_0))∨I_3~I_0	Performs a logical OR operation between the contents of a port specified by P3 to P0 and immediate data I3I2I1I0 and outputs the resulted sum to the port.	ZF	
Timer control instructions	WTTM0	Write timer 0	1 1 0 0	1 0 1 0	1	2	TIMER0←(M2(HL)), (AC)	Writes the contents of the M(HL) and the accumulator (AC) to the timer 0 reload register.		
	WTTM1	Write timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 0	2	2	TIMER1←(E), (AC)	Writes the contents of the E register and the accumulator (AC) to the timer 1 reload register.		
	RTIM0	Read timer 0	1 1 0 0	1 0 1 1	1	2	M2(HL), AC←(TIMER0)	Reads the contents of the timer 0 counter into the M2(HL) and the accumulator (AC).		
	RTIM1	Read timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 1	2	2	E, AC←(TIMER1)	Reads the contents of the timer 1 counter into the E register and the accumulator (AC).		
	START0	Start timer 0	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 0	2	2	Start timer 0 counter	Starts the timer 0 counter operation.		
	START1	Start timer 1	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 1	2	2	Start timer1 counter	Starts the timer 1 counter operation.		
	STOP0	Stop timer 0	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 0	2	2	Stop timer 0 counter	Stops the timer 0 counter operation.		
	STOP1	Stop timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 1	2	2	Stop timer1 counter	Stops the timer 1 counter operation.		

Instruction type	Mnemonics		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flags affected	Remarks
Interrupt control instructions	MSET	Set Interrupt Master Enable Flag	1 1 0 0 0 1 0 1	1 1 0 1 0 0 0 0	2	2	MSE←1	Sets the interrupt master enable flag.		
	MRESET	Reset Interrupt Master Enable Flag	1 1 0 0 1 0 0 1	1 1 0 1 0 0 0 0	2	2	MSE←0	Resets the interrupt master enable flag.		
	EIH i4	Enable interrupt high	1 1 0 0 0 1 0 1	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIH←(EDIH)∨i4	Sets the interrupt enable flag.		
	EIL i4	Enable interrupt low	1 1 0 0 0 1 0 0	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIL←(EDIL)∨i4	Sets the interrupt enable flag.		
	DIH i4	Disable interrupt high	1 1 0 0 1 0 0 1	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIH←(EDIH)∧$\overline{i4}$	Resets the interrupt enable flag.	ZF	
	DIL i4	Disable interrupt low	1 1 0 0 1 0 0 0	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIL←(EDIL)∧$\overline{i4}$	Resets the interrupt enable flag.	ZF	
	WTSP	Write SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 0	2	2	SP←(E), (AC)	Transfers the contents of the E register and accumulator (AC) to the stack area.		
	RSP	Read SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 1	2	2	E, AC←(SP)	Transfers the contents of the stack area to the E register and accumulator (AC).		
Standby control instructions	HALT .	HALT	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 0	2	2	HALT	Selects the HALT mode.		
	HOLD	HOLD	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 1	2	2	HOLD	Selects the HOLD mode.		
Serial I/O control instructions	STARTS	Start serial I/O	1 1 0 0 1 1 1 0	1 1 1 1 1 1 1 0	2	2	START SI/O	Starts the SIO operation mode.		
	WTSIO	Write serial I/O	1 1 0 0 1 1 1 0	1 1 1 1 1 1 1 1	2	2	SIO ←(E), (AC)	Writes the contents of the E register and accumulator (AC) to the SIO register.		
	RSIO	Read serial I/O	1 1 0 0 1 1 1 1	1 1 1 1 1 1 1 1	2	2	E, AC←(SIO)	Reads the contents of the SIO register into the E register and the accumulator (AC).		
Other instructions	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	A dummy instruction that is coded 00H and has no effect when executed. Just one machine cycle signal reaches the CPU.		
	SB i2	Select bank	1 1 0 0 1 1 0 0	1 1 1 1 0 0 I_1 I_0	2	2	PC13, PC12←I_1 I_0	Selects memory banks.		Usable only on LC66599